

### Description

The HSM6032 is the high cell density trenched N-ch MOSFETs, which provide excellent RDSON and gate charge for most of the synchronous buck converter applications.

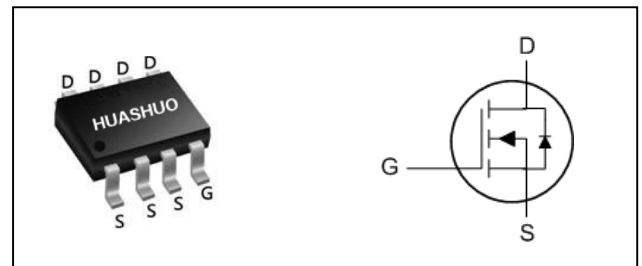
The HSM6032 meet the RoHS and Green Product requirement, 100% EAS guaranteed with full function reliability approved.

- Super Low Gate Charge
- 100% EAS Guaranteed
- Green Device Available
- Excellent CdV/dt effect decline
- Advanced high cell density Trench technology

### Product Summary

$V_{DS}$	60	V
$R_{DS(ON),max}$	8.5	m $\Omega$
$I_D$	13	A

### SOP8 Pin Configuration



### Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
$V_{DS}$	Drain-Source Voltage	60	V
$V_{GS}$	Gate-Source Voltage	$\pm 20$	V
$I_D@T_A=25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^1$	13	A
$I_D@T_A=100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^1$	8	A
$I_{DM}$	Pulsed Drain Current <sup>2</sup>	60	A
EAS	Single Pulse Avalanche Energy <sup>3</sup>	80	mJ
$I_{AS}$	Avalanche Current	40	A
$P_D@T_A=25^\circ C$	Total Power Dissipation <sup>4</sup>	2.7	W
$T_{STG}$	Storage Temperature Range	-55 to 150	$^\circ C$
$T_J$	Operating Junction Temperature Range	-55 to 150	$^\circ C$

### Thermal Data

Symbol	Parameter	Typ.	Max.	Unit
$R_{\theta JA}$	Thermal Resistance Junction-ambient <sup>1</sup> ( $t \leq 10S$ )	---	45	$^\circ C/W$
	Thermal Resistance Junction-ambient <sup>1</sup> (Steady State)	---	80	$^\circ C/W$



**Electrical Characteristics ( $T_J=25\text{ }^\circ\text{C}$ , unless otherwise noted)**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	60	---	---	V
$R_{DS(on)}$	Static Drain-Source On-Resistance <sup>2</sup>	$V_{GS}=10V, I_D=10A$	---	---	8.5	$m\Omega$
		$V_{GS}=4.5V, I_D=8A$	---	---	12	$m\Omega$
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS}=V_{DS}, I_D=250\mu A$	1.2	---	2.5	V
$I_{DSS}$	Drain-Source Leakage Current	$V_{DS}=48V, V_{GS}=0V, T_J=25^\circ C$	---	---	1	$\mu A$
		$V_{DS}=48V, V_{GS}=0V, T_J=55^\circ C$	---	---	5	
$I_{GSS}$	Gate-Source Leakage Current	$V_{GS}=\pm 20V, V_{DS}=0V$	---	---	$\pm 100$	nA
$g_{fs}$	Forward Transconductance	$V_{DS}=5V, I_D=10A$	---	50	---	S
$Q_g$	Total Gate Charge (10V)	$V_{DS}=48V, V_{GS}=10V, I_D=10A$	---	57	---	nC
$Q_{gs}$	Gate-Source Charge		---	8.7	---	
$Q_{gd}$	Gate-Drain Charge		---	14	---	
$T_{d(on)}$	Turn-On Delay Time	$V_{DD}=30V, V_{GS}=10V, R_G=3.3\Omega, I_D=10A$	---	16.2	---	ns
$T_r$	Rise Time		---	41.2	---	
$T_{d(off)}$	Turn-Off Delay Time		---	56.4	---	
$T_f$	Fall Time		---	16.2	---	
$C_{iss}$	Input Capacitance	$V_{DS}=25V, V_{GS}=0V, f=1MHz$	---	3307	---	pF
$C_{oss}$	Output Capacitance		---	201	---	
$C_{rss}$	Reverse Transfer Capacitance		---	151	---	

**Diode Characteristics**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$I_S$	Continuous Source Current <sup>1,5</sup>	$V_G=V_D=0V, \text{ Force Current}$	---	---	10	A
$I_{SM}$	Pulsed Source Current <sup>2,5</sup>		---	---	60	A
$V_{SD}$	Diode Forward Voltage <sup>2</sup>	$V_{GS}=0V, I_S=1A, T_J=25^\circ C$	---	---	1.2	V
$t_{rr}$	Reverse Recovery Time	$I_F=10A, dI/dt=100A/\mu s, T_J=25^\circ C$	---	24	---	nS
$Q_{rr}$	Reverse Recovery Charge		---	15	---	nC

Note :

- 1.The data tested by surface mounted on a 1 inch<sup>2</sup> FR-4 board with 2OZ copper.
- 2.The data tested by pulsed , pulse width  $\leq 300\mu s$  , duty cycle  $\leq 2\%$
- 3.The EAS data shows Max. rating . The test condition is  $V_{DD}=50V, V_{GS}=10V, L=0.1mH, I_{AS}=40A$
- 4.The power dissipation is limited by 150 $^\circ\text{C}$  junction temperature
- 5.The data is theoretically the same as  $I_D$  and  $I_{DM}$  , in real applications , should be limited by total power dissipation.



Typical Characteristics

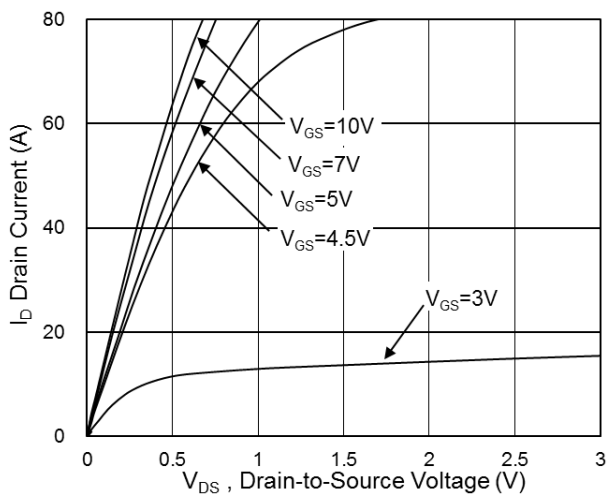


Fig.1 Typical Output Characteristics

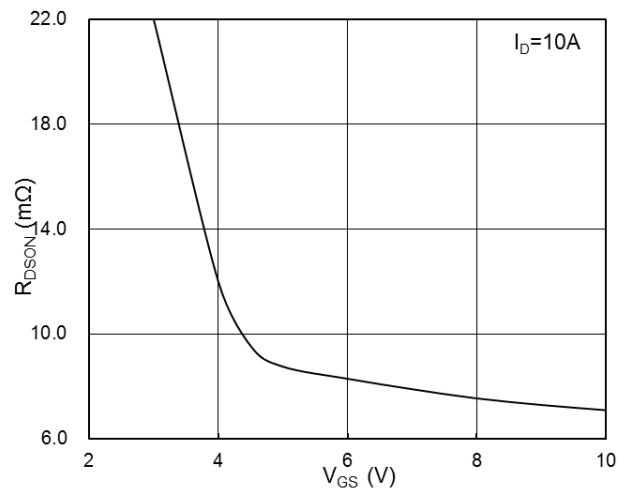


Fig.2 On-Resistance v.s Gate-Source Voltage

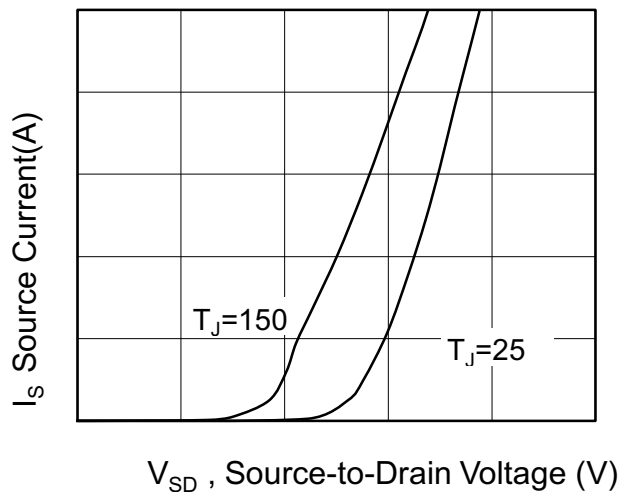


Fig.3 Forward Characteristics of Reverse

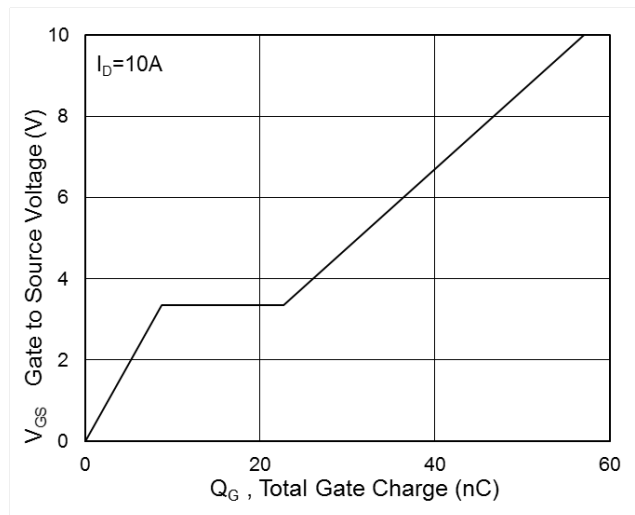


Fig.4 Gate-Charge Characteristics

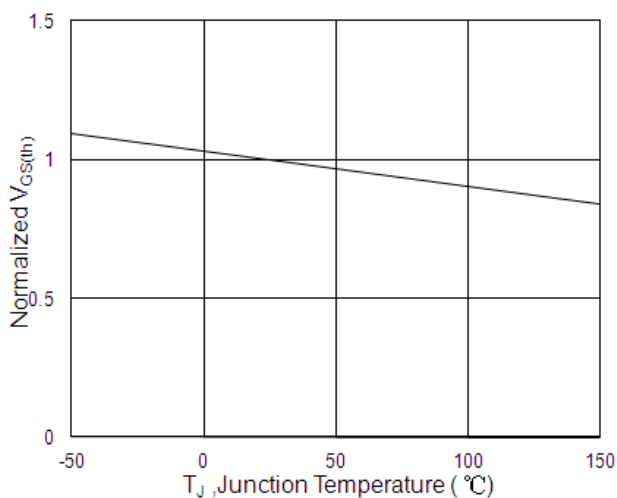


Fig.5 Normalized  $V_{GS(th)}$  vs.  $T_J$

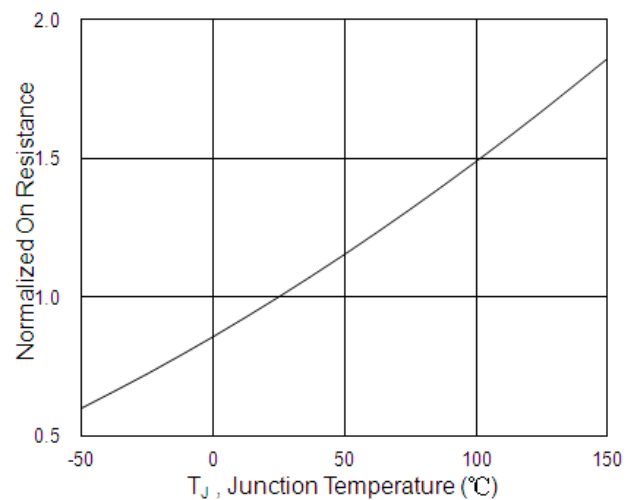
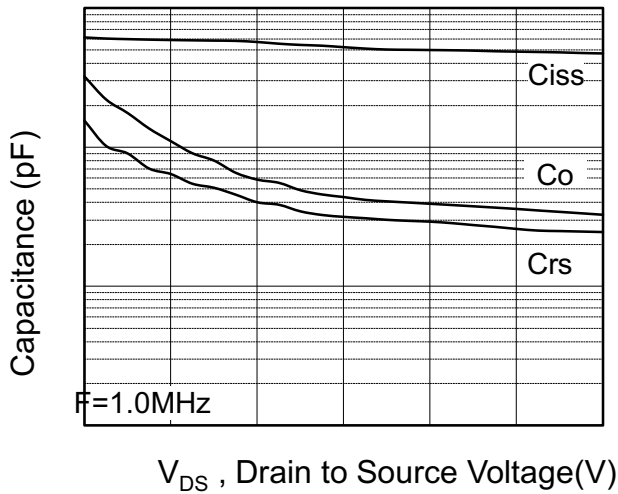
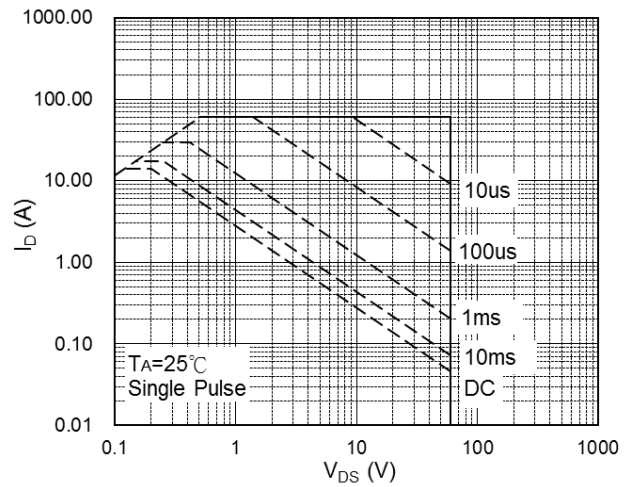


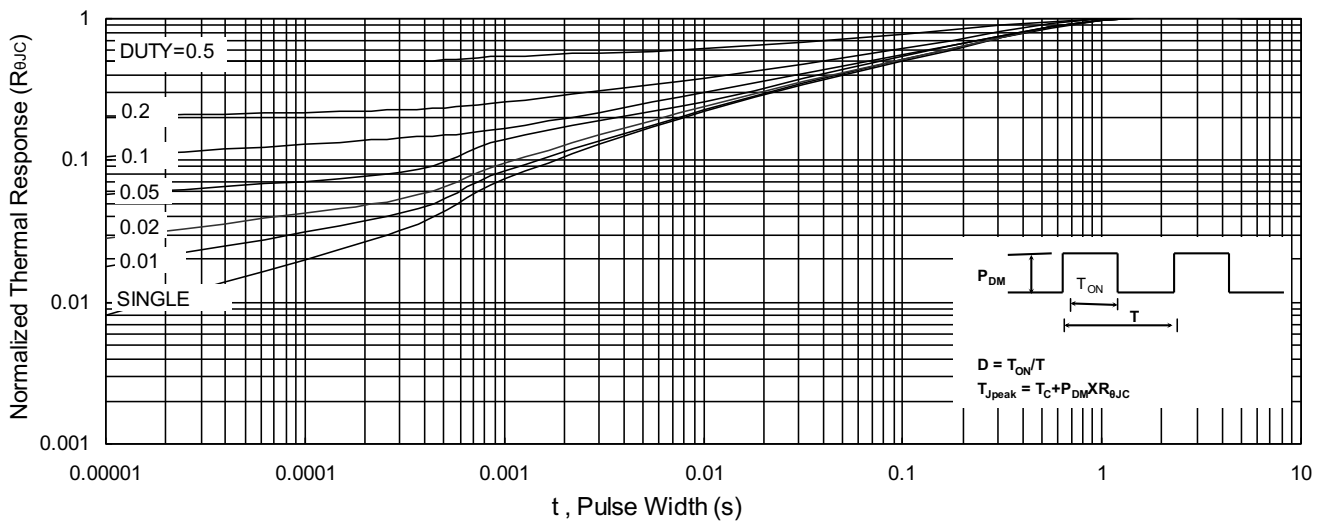
Fig.6 Normalized  $R_{DS(on)}$  vs.  $T_J$



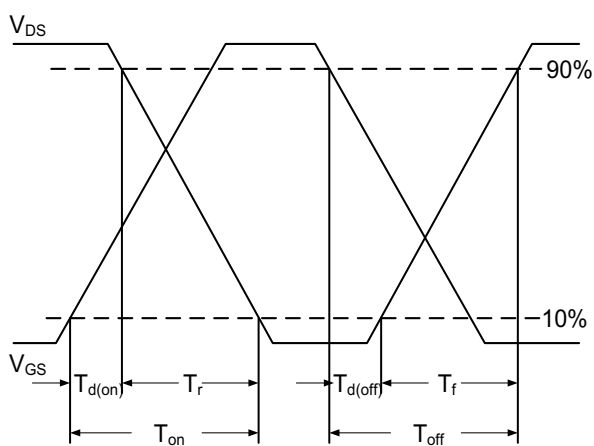
**Fig.7 Capacitance**



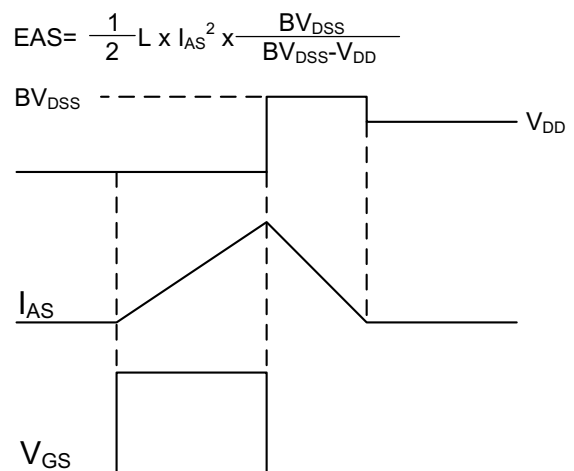
**Fig.8 Safe Operating Area**



**Fig.9 Normalized Maximum Transient Thermal Impedance**



**Fig.10 Switching Time Waveform**



**Fig.11 Unclamped Inductive Switching**