Ultra Fast High PSRR Low Noise CMOS Voltage Regulators

CJ6221 Series

■ INTRODUCTION

The CJ6221 series are a group of positive voltage regulators manufactured by CMOS technologies with high ripple rejection, ultra-low noise, low power consumption and low dropout voltage, which can prolong battery life in portable electronics. The CJ6221 series work with low-ESR ceramic capacitors, reducing the amount of board space necessary for power applications. The CJ6221 series consume less than 0.1μA in shutdown mode and have fast turn-on time less than 50μS.The series are very suitable for the battery-powered equipment, such as RF applications and other systems requiring a quiet voltage source.

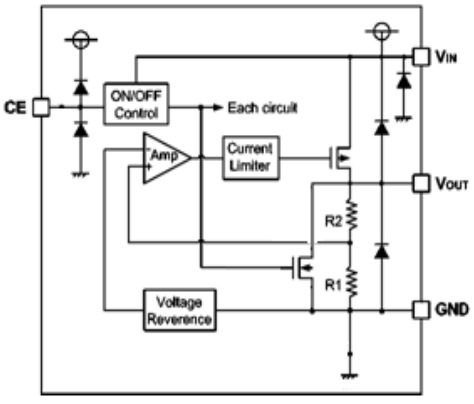
■ FEATURES

- Low Output Noise：
  $40\mu V_{RMS}$(10Hz~100kHz)
- Low Dropout Voltage：50mV@100mA
- Low Quiescent Current：30μA
- High Ripple Rejection：80dB@1KHz
- Excellent Line and Load Transient Response
- Operating Voltage Range：1.8V～6.0V
- Output Voltage Range：0.8V ~ 5.0V
- High Accuracy：±2％（Typ.）
- Built-in Current Limiter, Short-Circuit Protection
- TTL- Logic-Controlled Shutdown Input

■ APPLICATIONS

- Cellular and Smart Phones
- Laptop, Palmtops and PDA
- Digital Still and Video Cameras
- Portable Audio Video Equipments
- Radio control systems
- Battery-Powered Equipments

■ BLOCK DIAGRAM



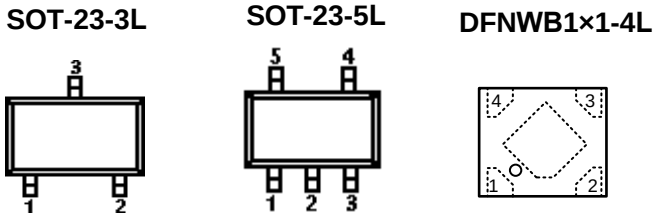
■ ORDER INFORMATION

CJ6221①②③④

DESIGNATOR	SYMBOL	DESCRIPTION
①	A	Standard
	B	High Active, pull-down resistor built in, with C_{OUT} discharge resistor
②③	Integer	Output Voltage e.g.1.8V=②:1, ③:8
④	M	Package:SOT-23-3L/5L
	F	Package:DFNWB1x1-4L

■ PIN CONFIGURATION

SOT-23-3L **SOT-23-5L** **DFNWB1×1-4L**



SOT-23-3L

PIN NUMBER	SYMBOL	FUNCTION
M		
1	V_{SS}	Ground
2	V_{OUT}	Output
3	V_{IN}	Power Input Pin

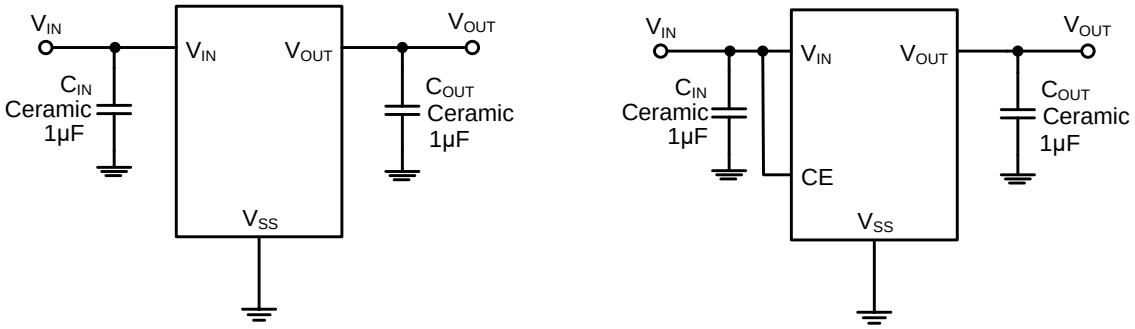
SOT-23-5L

PIN NUMBER	SYMBOL	FUNCTION
M		
1	V_{IN}	Power Input Pin
2	V_{SS}	Ground
3	CE	Chip Enable Pin
4	NC	No Connection
5	V_{OUT}	Output Pin

DFNWB1×1-4L

PIN NUMBER	SYMBOL	FUNCTION
F		
1	V_{OUT}	Output Pin
2	V_{SS}	Ground
3	CE	Chip Enable Pin
4	V_{IN}	Power Input Pin

■ TYPICAL APPLICATION



■ ABSOLUTE MAXIMUM RATINGS(1)

(Unless otherwise specified, T_A=25°C)

PARAMETER		SYMBOL	RATINGS	UNITS
Input Voltage(2)		V_{IN}	-0.3~7	V
Output Voltage(2)		V_{OUT}	-0.3~V_{IN}+0.3	V
Output Current		I_{OUT}	700	mA
Power Dissipation	SOT-23-3L/SOT-23-5L	P_D	0.4	W
	DFNWB1×1-4L		0.3	W
Operating free air temperature range		T_A	-40~85	°C
Operating Junction Temperature Range(3)		T_j	-40~125	°C
Storage Temperature		T_{stg}	-40~125	°C
Lead Temperature(Soldering, 10 sec)		T_{solder}	260	°C
ESD rating(4)		Human Body Model(HBM)	2	kV
		Machine Model(MM)	200	V

(1) Stresses beyond those listed under *absolute maximum ratings may* cause permanent damage to the device. These are stress ratingsonly, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operatingconditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods my affect device reliability.

(2)All voltages are with respect to network ground terminal.

(3)This IC includes overtemperature protection that is intended toprotect the device during momentary overload. Junction temperature willexceed 125°C when overtemperature protection is active. Continuousoperation above the specified maximum operating junction temperaturemay impair device reliability.

(4)ESD testing is performed according to the respective JESD22 JEDEC standard.

The human body model is a 100 pF capacitor discharged through a 1.5kΩ resistor into each pin. The machine model is a 200pFcapacitor discharged directly into each pin.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	MIN.	NOM.	MAX.	UNITS
Supply voltage at V_{IN}	1.8		6	V
Operating junction temperature range, T_j	0		125	°C
Operating free air temperature range, T_A	0		85	°C

Electrical Characteristics

(V_{IN}=V_{OUT}+1V, C_{IN}=C_{OUT}=1μF, T_A=25℃,unless otherwise specified)

PARAMETER		SYMBOL	CONDITIONS	MIN.	TYP.(6)	MAX.	UNITS
Output Voltage		$V_{OUT}(E)$(7)	I_{OUT}=1mA	V_{OUT}(8) *0.98	V_{OUT}(8)	V_{OUT}(8) *1.02	V
Supply Current		I_{SS}	I_{OUT}=0		30	60	μA
Standby Current		I_{STBY}	CE = V_{SS}		0.1	1	μA
Output Current		I_{OUT}	V_{OUT}≥1.0V	500	700		mA
			V_{OUT}＜1.0V	300	500		
Dropout Voltage		V_{DO}(9)	I_{OUT} =100mA V_{OUT}≥3.3V		50		mV
			V_{OUT}≤1.1V		700		
Load Regulation		ΔV_{OUT}	V_{IN}= V_{OUT} +1V, 1mA≤I_{OUT}≤100mA		1		mV
Line Regulation		$\frac{\Delta V_{OUT}}{V_{OUT} \times \Delta V_{IN}}$	I_{OUT} =10mA V_{OUT} +1V≤V_{IN}≤6V			0.3	%/V
Output Voltage Temperature Characteristics		$\frac{\Delta V_{OUT}}{\Delta T \times V_{OUT}}$	I_{OUT} =10mA -40≤T≤+85		50		ppm
Short Current		I_{Short}	V_{OUT} =V_{SS}		50		mA
Input Voltage		V_{IN}	—	1.8		6.0	V
Power Supply Rejection Rate	100Hz	PSRR	I_{OUT}=50mA		75		dB
	1kHz				80		
	10kHz				70		
CE "High" Voltage		V_{CE}“H”		1.5		V_{IN}	V
CE "Low" Voltage		V_{CE}“L”				0.3	V
C_{OUT} Auto-Discharge Resistance		$R_{DISCHRG}$	V_{IN}=5V, V_{OUT}=3.0V, V_{CE}=V_{SS}		60		Ω
Thermal Shutdown		T_{SD}			140		℃
Thermal Shutdown		ΔT_{SD}			20		℃

(6) Typical numbers are at 25°C and represent the mostlikely norm.

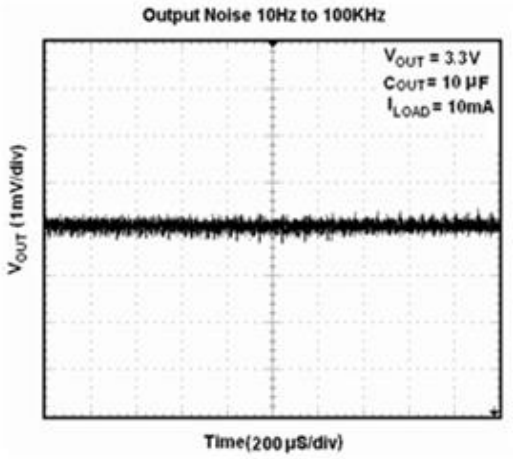
(7)V_{OUT}(E) : Effective Output Voltage (Ie. The output voltage when V_{IN}= (V_{OUT} +1.0V) andmaintain acertain I_{OUT} Value).

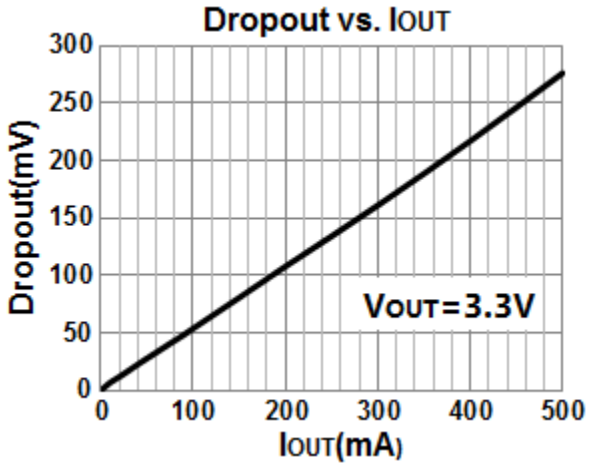
(8)V_{OUT}: Specified Output Voltage.

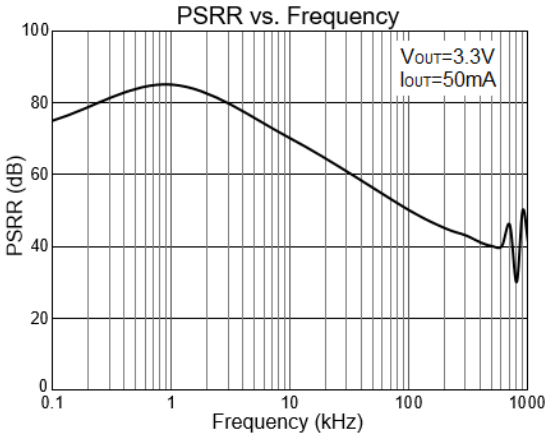
(9)V_{DO} : The Difference Of Output Voltage And Input Voltage When Input Voltage Is Decreased Gradually Till Output Voltage Equals To 98% Of V_{OUT} (E).

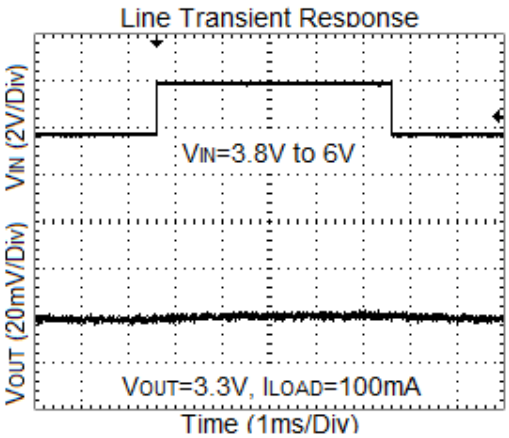
Typical Characteristics

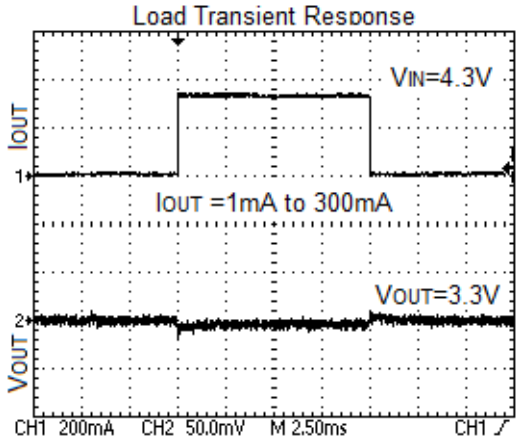
(V_{CE}=V_{IN}=V_{OUT}+1V, C_{IN}=C_{OUT}=1μF，T_A=25℃,unless otherwise specified)

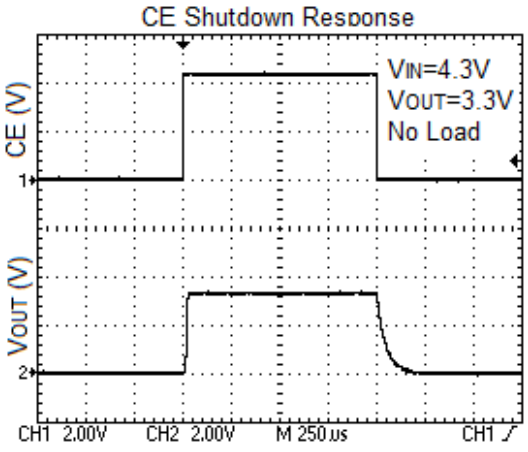












C_{OUT} Auto-Discharge Function

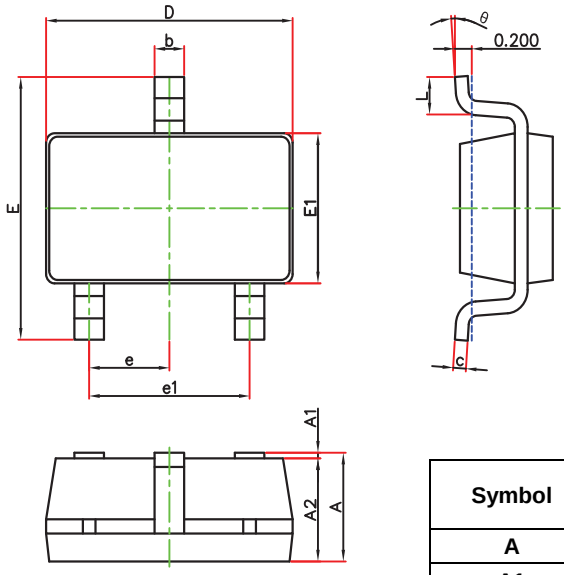
CJ6221B series can discharge the electric charge in the output capacitor (C_{OUT}), when a low signal to the CE pin, which enables a whole IC circuit turn off, is inputted via the N-channel transistor located between the V_{OUT} pin and the V_{SS} pin (cf. BLOCK DIAGRAM). The C_{OUT} auto-discharge resistance value is set at60Ω(V_{OUT}=3.0V @ V_{IN}=5.0V at typical). The discharge time of the output capacitor (C_{OUT}) is set by the C_{OUT} auto-discharge resistance (R) and the output capacitor (C_{OUT}). By setting time constant of a C_{OUT} auto-discharge resistance value [$R_{DISCHRG}$] and an output capacitor value (C_{OUT}) as τ(τ=C x $R_{DISCHRG}$), the output voltage after discharge via the N-channel transistor is calculated by the following formulas.

$$V = V_{OUT(E)} \times e^{-t/\tau},\ or\ t=\tau ln\ (\ V / V_{OUT(E)}\ )$$

(V : Output voltage after discharge, $V_{OUT(E)}$: Output voltage, t: Discharge time,

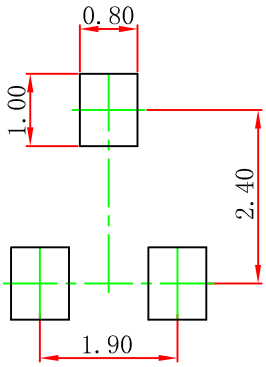
τ: C_{OUT} auto-discharge resistance $R_{DISCHRG}$×Output capacitor (C_{OUT}) value C)

SOT-23-3L Package Outline Dimensions



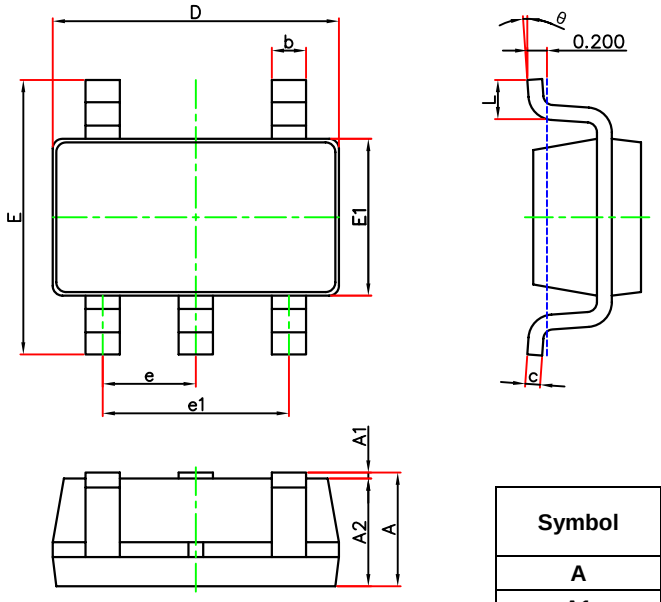
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	2.650	2.950	0.104	0.116
E1	1.500	1.700	0.059	0.067
e	0.950(BSC)		0.037(BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

SOT-23-3L Suggested Pad Layout



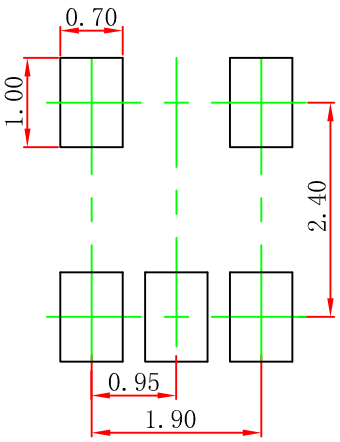
Note:
1.Controlling dimension:in millimeters.
2.General tolerance:± 0.05mm.
3.The pad layout is for reference purposes only.

SOT-23-5L Package Outline Dimensions



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	2.650	2.950	0.104	0.116
E1	1.500	1.700	0.059	0.067
e	0.950(BSC)		0.037(BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

SOT-23-5L Suggested Pad Layout



Note:
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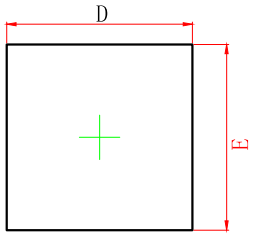
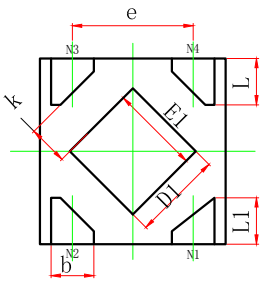
2.General tolerance:± 0.05mm.
3.The pad layout is for reference purposes only.

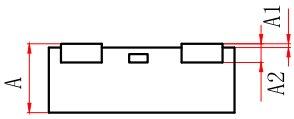
DFNWB1*1-4L Package Outline Dimensions



TOP VIEW



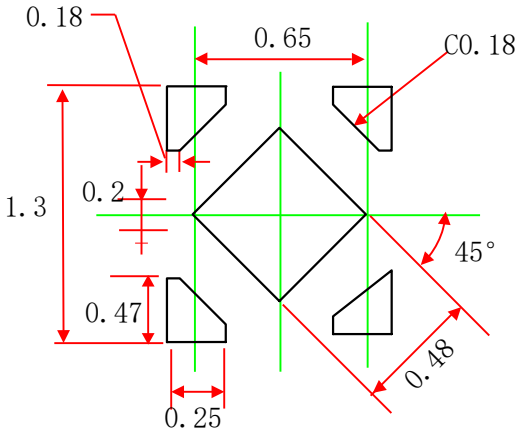
BOTTOM VIEW



SIDE VIEW

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.320	0.400	0.013	0.016
A1	0.000	0.050	0.000	0.002
A2	0.100 REF.		0.004 REF.	
D	0.950	1.050	0.037	0.041
E	0.950	1.050	0.037	0.041
D1	0.430	0.530	0.017	0.021
E1	0.430	0.530	0.017	0.021
k	0.150MIN.		0.006MIN.	
b	0.180	0.280	0.007	0.011
e	0.650TYP.		0.026TYP.	
L	0.200	0.300	0.008	0.012
L1	0.200	0.300	0.008	0.012

DFNWB1*1-4L Suggested Pad Layout



Note:
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2.General tolerance:±0.05mm.
3.The pad layout is for reference purposes only.

DISCLAIMER

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