

# 600KHz, 18V, 2.0A Synchronous Step-Down Converter

## FEATURES

- High Efficiency: Up to 94%(@5V)
- 600KHz Frequency Operation
- 2.0A Output Current
- No Schottky Diode Required
- 3.5V to 18V Input Voltage Range
- 0.6V Reference
- Slope Compensated Current Mode Control for Excellent Line and Load Transient Response
- Integrated internal compensation
- Stable with Low ESR Ceramic Output Capacitors
- Over Current Protection with Hiccup-Mode
- Input overvoltage protection(OVP)
- Thermal Shutdown
- Inrush Current Limit and Soft Start
- Available in SOT23-6 Package
- -40°C to +85°C Temperature Range

## GENERAL DESCRIPTION

The STI3470 is a fully integrated, high-efficiency 2.0A synchronous rectified step-down converter. The STI3470 operates at high efficiency over a wide output current load range.

This device offers two operation modes, PWM control and PFM Mode switching control, which allows a high efficiency over the wider range of the load.

The STI3470 requires a minimum number of readily available standard external components and is available in a 6-pin SOT23 ROHS compliant package.

## APPLICATIONS

- Distributed Power Systems
- Digital Set Top Boxes
- Flat Panel Television and Monitors
- Notebook computer
- Wireless and DSL Modems

## TYPICAL APPLICATION

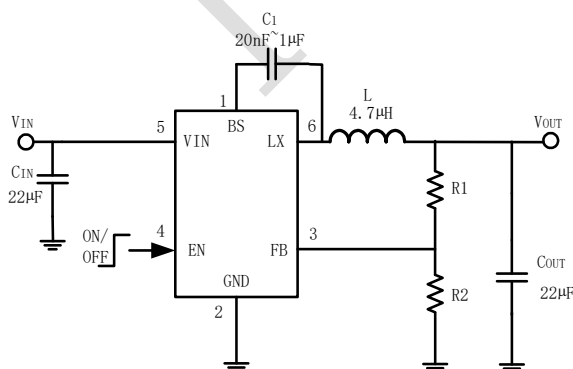
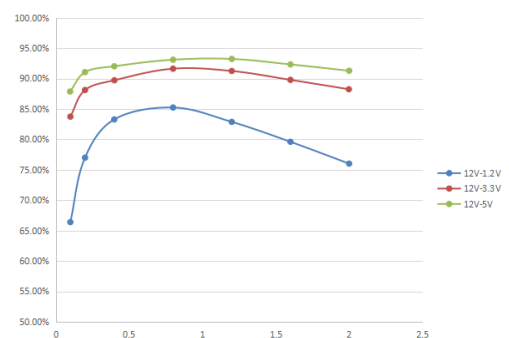


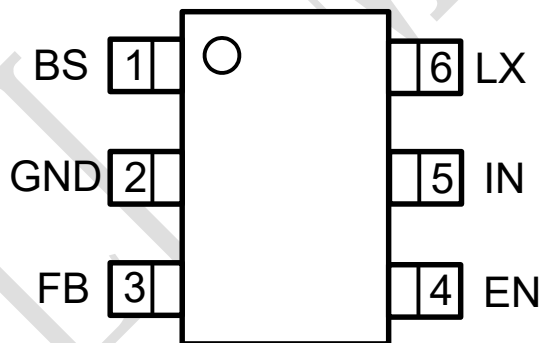
Figure 1. Basic Application Circuit



2. Efficiency(%) vs. Load Current(A)

**ABSOLUTE MAXIMUM RATINGS** (Note 1)

Parameter	Value	Unit
Input Supply Voltage ,EN	-0.3~23	V
LX Voltages	-0.3~23	V
FB Voltage	-0.3~6	V
BS Voltage	-0.6~25	V
Storage Temperature Range	-65~150	°C
Junction Temperature <sup>(Note2)</sup>	160	°C
Power Dissipation	600	mW
Lead Temperature(Soldering,10s)	260	°C

**PACKAGE/ORDER INFORMATION**


SOT23-6

**Top Mark: S47XXX (S47: Device Code, XXX: Inside Code)**

Part Number	Package	Top mark	Quantity/ Reel
STI3470	SOT23-6	S47XXX	3000

## PIN FUNCTIONS

Pin	Name	Function
1	BS	Bootstrap. A capacitor connected between LX and BST pins is required to form a floating supply across the high-side switch driver.
2	GND	Ground
3	FB	Adjustable version feedback input. Connect FB to the center point of the external resistor divider.
4	EN	Drive this pin to a logic-high to enable the IC. Drive to a logic-low to disable the IC and Not floating.
5	IN	Power supply Pin
6	LX	Switching Pin

## ESD RATING

Items	Description	Value	Unit
V <sub>ESD</sub>	Human Body Model for all pins	±2000	V

JEDEC specification JS-001

## RECOMMENDED OPERATING CONDITIONS

Items	Description	Min	Max	Unit
Voltage Range	IN	3.5	18	V
TA	Operating Temperature Range	-40	85	°C

## ELECTRICAL CHARACTERISTICS (Note 3)

( $V_{IN}=12V$ ,  $V_{OUT}=5V$ ,  $T_A = 25^{\circ}C$ , unless otherwise noted.)

Parameter	Conditions	Min	Typ	Max	Unit
Input Voltage Range		3.5		18	V
OVP Threshold			19		V
UVLO Threshold		3.0			V
Supply Current in Operation	$V_{EN}=2.0V$ , $V_{FB}=1.1V$		0.4	0.6	mA
Supply Current in Shutdown	$V_{EN}=0$		1		uA
Regulated Feedback Voltage	$T_A = 25^{\circ}C$ , $3.5V \leq V_{IN} \leq 18V$	0.588	0.6	0.612	V
High-Side Switch On-Resistance			120		m $\Omega$
Low-Side Switch On-Resistance			80		m $\Omega$
High-Side Switch Leakage Current	$V_{EN}=0V$ , $V_{LX}=0V$		0	10	uA
Upper Switch Current Limit	Minimum Duty Cycle	2.5			A
Oscillation Frequency	$V_{FB}=0.6$		600		KHz
Maximum Duty Cycle	$V_{FB}=0.6$		95		%
EN Rising Threshold		1.50			V
EN Falling Threshold				0.30	V
Minimum On-Time			60		nS
Thermal Shutdown			160		$^{\circ}C$

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2:  $T_J$  is calculated from the ambient temperature  $T_A$  and power dissipation  $P_D$  according to the following formula:  $T_J = T_A + (P_D) \times (250^{\circ}C/W)$ .

Note 3: 100% production test at  $+25^{\circ}C$ . Specifications over the temperature range are guaranteed by design and characterization.

Note 4: Dynamic supply current is higher due to the gate charge being delivered at the switching frequency

## OPERATION

### Internal Regulator

The STI3470 is a current mode step down DC/DC converter that provides excellent transient response with no extra external compensation components. This device contains an internal, low resistance, high voltage power MOSFET, and operates at a high 600K operating frequency to ensure a compact, high efficiency design with excellent AC and DC performance.

### Error Amplifier

The error amplifier compares the FB pin voltage with the internal FB reference (VFB) and outputs a current proportional to the difference between the two. This output current is then used to charge or discharge the internal compensation network to form the COMP voltage, which is used to control the power MOSFET current. The optimized internal compensation network minimizes the external component counts and simplifies the control loop design.

### Internal Soft-Start

The soft-start is implemented to prevent the converter output voltage from overshooting during startup. When the chip starts, the internal circuitry generates a soft-start voltage (SS) ramping up from 0V to 0.6V. When it is lower than the internal reference (REF), SS overrides REF so the error amplifier uses SS as the reference. When SS is higher than REF, REF regains control. The SS time is internally fixed to 1ms.

### Over-Current-Protection and Hiccup

The STI3470 has cycle-by-cycle over current limit when the inductor current peak value exceeds the set current limit threshold. Meanwhile, output voltage starts to drop until FB is below the Under-Voltage (UV) threshold, typically 30% below the reference. Once a UV is triggered, the STI3470 enters hiccup mode to periodically restart the part. This protection mode is especially useful when the output is dead-short to ground. The average short circuit current is greatly reduced to alleviate the thermal issue and to protect the regulator. The STI3470 exits the hiccup mode once the over current condition is removed.

### Startup and Shutdown

If both VIN and EN are higher than their appropriate thresholds, the chip starts. The reference block starts first, generating stable reference voltage and currents, and then the internal regulator is enabled. The regulator provides stable supply for the remaining circuitries. Three events can shut down the chip: EN low, VIN low and thermal shutdown. In the shutdown procedure, the signaling path is first blocked to avoid any fault triggering. The COMP voltage and the internal supply rail are then pulled down. The floating driver is not subject to this shutdown command.

## FUNCTIONAL BLOCK DIAGRAM

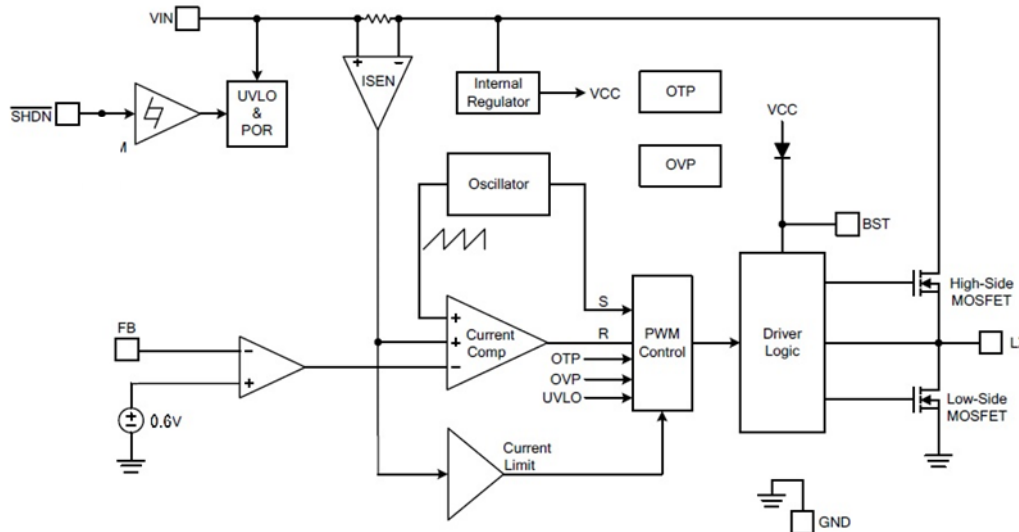


Figure 3. STI3470 Block Diagram

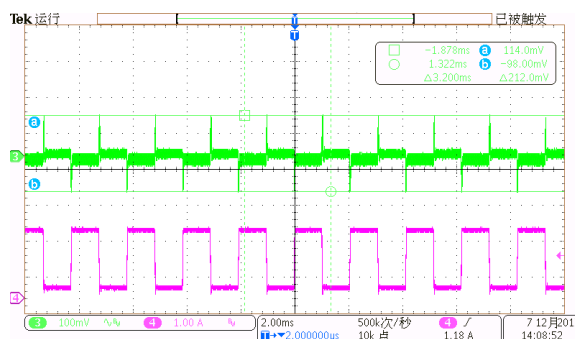
## FUNCTIONAL TEST

Test condition:  $V_{in}=12V, V_{out}=3.3V$ ;

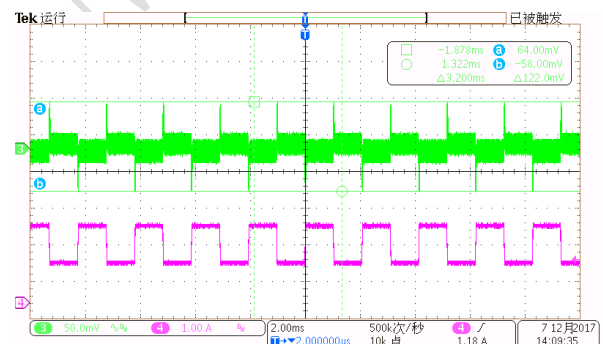
### 1. Load Dynamic Response

10%~90% load

50%~100% load



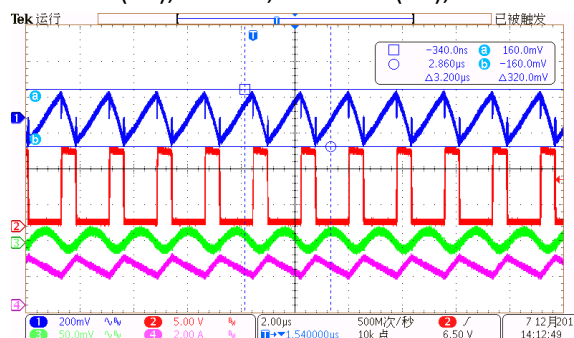
Load transient(0.2A-1.8A-0.2A)



Load transient(1A-2A-1A)

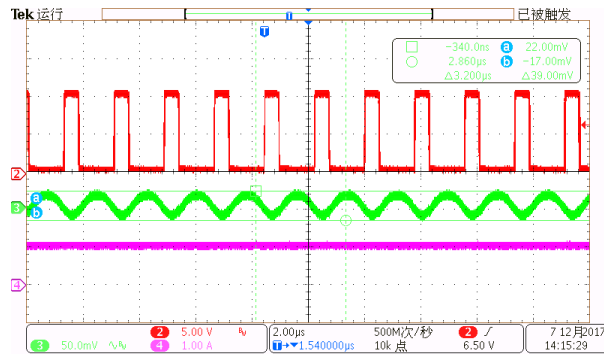
### 2. Input/output ripple, $I_{out}=\text{full load}$

CH1:VIN(AC);CH2:SW;CH3:VOUT(AC);CH4:Isw



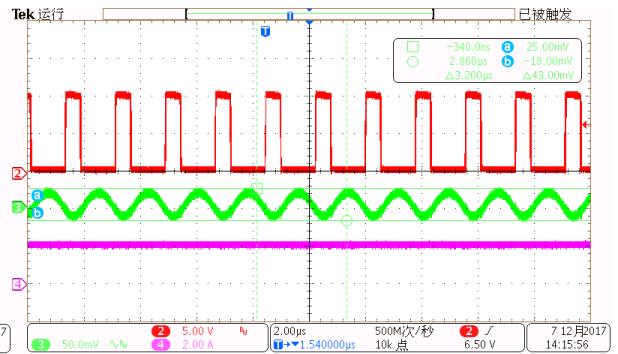
### 3.Vout ripple and Switching waveform

CH2:SW;CH3:VOUT(AC);CH4:Iout



Iout=50% load

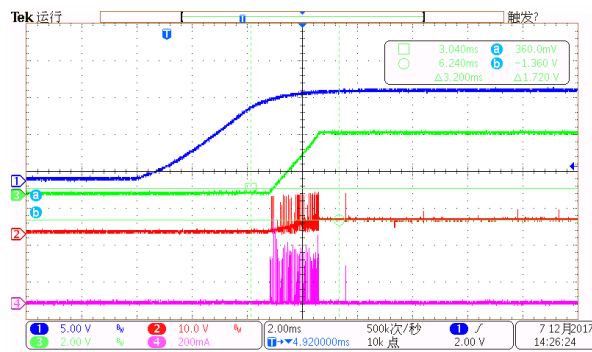
CH2:SW;CH3:VOUT(AC);CH4:Iout



Iout=100% load

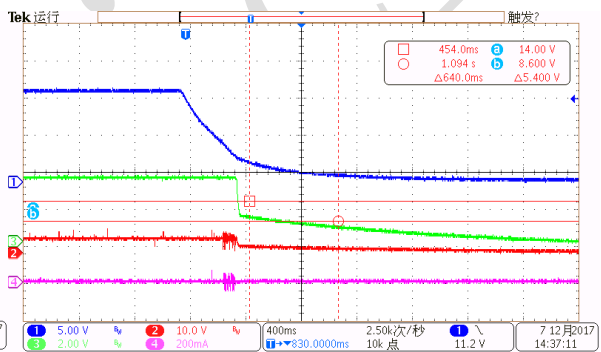
### 4.Power on/off:

CH1:VIN;CH2:SW;CH3:VOUT;CH4:Isw



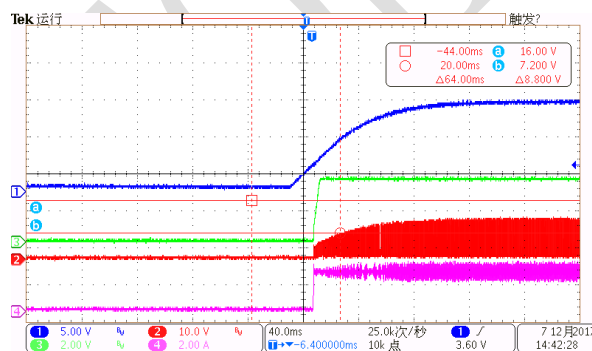
Power on, Iout= 0A

CH1:VIN;CH2:SW;CH3:VOUT;CH4:Isw



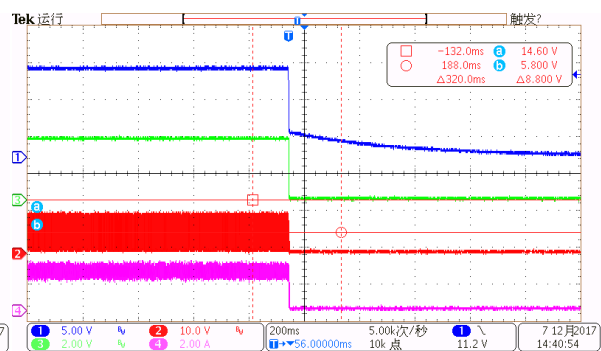
Power off, Iout= 0A

CH1:VIN;CH2:SW;CH3:VOUT;CH4:Isw



Power on, Iout= 2A

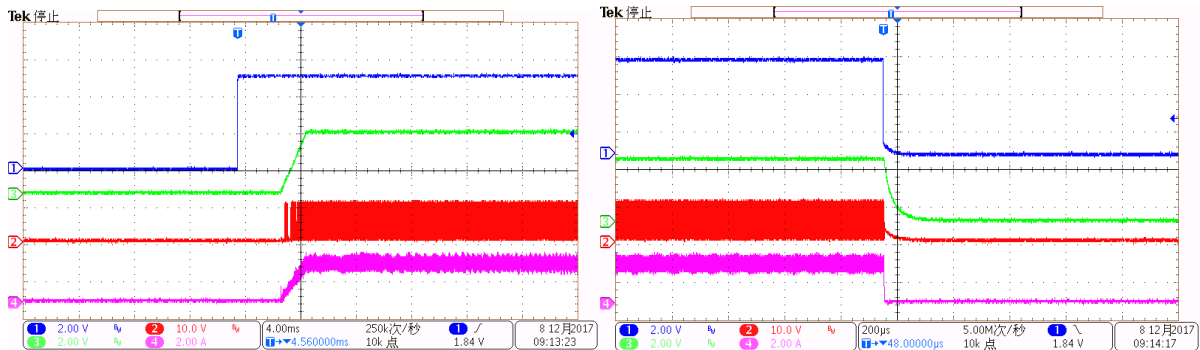
CH1:VIN;CH2:SW;CH3:VOUT;CH4:Isw



Power off, Iout= 2A

## 5.EN on/off:

CH1:EN;CH2:VOUT;CH3:SW;CH4:Isw



EN on , Iout= 2A

EN off , Iout= 2A

## APPLICATION INFORMATION

## Setting the Output Voltage

The external resistor divider is used to set the output voltage (see Typical Application on page 1). The feedback resistor R1 also sets the feedback loop bandwidth with the internal compensation capacitor. Choose R1 to be around 51kΩ for optimal transient response. R2 is then given by:

$$R_2 = \frac{R_1}{V_{out} / V_{FB} - 1}$$

Vout	R1(KΩ)	R2(KΩ)
5.1V	51	6.8
3.3V	51	11.3
1.8V	51	25.5
1.55V	51	33
1.25V	51	47
1.20V	51	51
1.05V	33	47

## Inductor Selection

A 4.7μH to 22μH inductor with a DC current rating of at least 25% percent higher than the maximum load current is recommended for most applications. For highest efficiency, the inductor DC resistance should be less than 15mΩ. For most designs, the inductance value can be derived from the following equation.

$$L = \frac{V_{out} \times (V_{in} - V_{out})}{V_{in} \times \Delta I_L \times f_{OSC}}$$

Where ΔIL is the inductor ripple current. Choose inductor ripple current to be approximately 30% if the maximum load current, 2A. The maximum inductor peak current is:

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2}$$

Under light load conditions below 100mA, larger inductance is recommended for improved efficiency.



## Output Capacitor Selection

The output capacitor (C2) is required to maintain the DC output voltage. Ceramic, tantalum, or low ESR electrolytic capacitors are recommended. Low ESR capacitors are preferred to keep the output voltage ripple low. The output voltage ripple can be estimated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_s \times L} \times \left[ 1 - \frac{V_{OUT}}{V_{IN}} \right] \times \left[ R_{ESR} + \frac{1}{8 \times f_s \times C_2} \right]$$

Where L is the inductor value and RESR is the equivalent series resistance (ESR) value of the output capacitor. In the case of ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance. The output voltage ripple is mainly caused by the capacitance. For simplification, the output voltage ripple can be estimated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_s^2 \times L \times C_2} \times \left[ 1 - \frac{V_{OUT}}{V_{IN}} \right]$$

In the case of tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated to:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_s \times L} \times \left[ 1 - \frac{V_{OUT}}{V_{IN}} \right] \times R_{ESR}$$

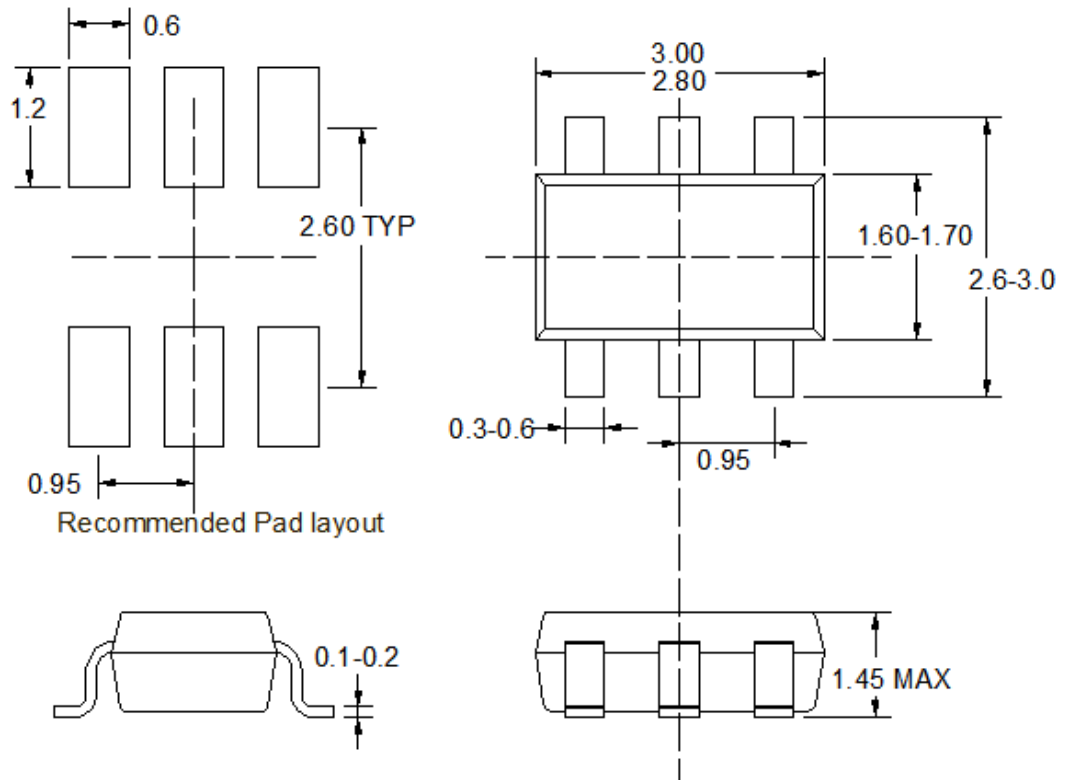
The characteristics of the output capacitor also affect the stability of the regulation system. The STI3470 can be optimized for a wide range of capacitance and ESR values.

## Layout Consideration

PCB layout is very important to achieve stable operation. It is highly recommended to duplicate EVB layout for optimum performance. If change is necessary, please follow these guidelines and take Figure 4 for reference.

- 1) Keep the path of switching current short and minimize the loop area formed by Input capacitor, high-side MOSFET and low-side MOSFET.
- 2) Bypass ceramic capacitors are suggested to be put close to the Vin Pin.
- 3) Ensure all feedback connections are short and direct. Place the feedback resistors and compensation components as close to the chip as possible.
- 4) VOUT, LX away from sensitive analog areas such as FB.
- 5) Connect IN, LX, and especially GND respectively to a large copper area to cool the chip to improve thermal performance and long-term reliability.

## PACKAGE INFORMATION



SOT23-6

Note:

- 1) All dimensions are in millimeters.
- 2) Package length does not include mold flash, protrusion or gate burr.
- 3) Package width does not include interlead flash or protrusion.
- 4) Lead popularity (bottom of leads after forming) shall be 0.10 millimeters max.
- 5) Pin 1 is lower left pin when reading top mark from left to right