Lonten N-channel 650V, 25A, 0.125Ω LonFET™ Power MOSFET

Description

LonFET™ Power MOSFET is fabricated using **advanced super junction** technology. The resulting device has extremely low on resistance, making it especially suitable for applications which require superior power density and outstanding efficiency.

Features

- Ultra low $R_{DS(on)}$
- Ultra low gate charge (typ. Q_g = 43nC)
- 100% UIS tested
- RoHS compliant

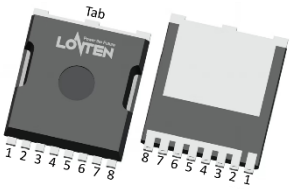
Applications

- Power factor correction (PFC).
- Switched mode power supplies (SMPS).
- Uninterruptible power supply (UPS).

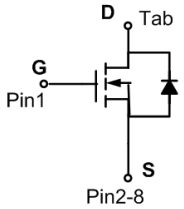
Product Summary

V_{DS} @ $T_{j,max}$	700V
$R_{DS(on),max}$	0.125Ω
I_{DM}	75A
$Q_{g,typ}$	43nC

Pin Configuration



TOLL



N-Channel MOSFET

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	650	V
Continuous drain current (T_C = 25°C)	I_D	25	A
(T_C = 100°C)		15.8	A
Pulsed drain current [1]	I_{DM}	75	A
Gate-Source voltage	V_{GSS}	±30	V
Avalanche energy, single pulse [2]	E_{AS}	688	mJ
Power Dissipation	P_D	204	W
Operating and Storage Temperature Range	T_J, T_{STG}	-55 to +150	°C
Continuous diode forward current	I_S	25	A
Diode pulse current	$I_{S,pulse}$	75	A

Thermal Characteristics

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	0.61	°C/W
Thermal Resistance, Junction-to-Ambient, minimal footprint [3]	$R_{\theta JA}$	62	°C/W
Soldering temperature, wavesoldering only allowed at leads. (1.6mm from case for 10s)	T_{sold}	260	°C

Package Marking and Ordering Information

Device	Device Package	Marking	Units/Reel
LST65R125HT	TOLL	LST65R125HT	2000

Electrical Characteristics

T_c = 25°C unless otherwise noted

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Static characteristics						
Drain-source breakdown voltage	BV_{DSS}	V_{GS}=0 V, I_D=0.25 mA	650	-	-	V
Gate threshold voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=0.25mA	2.5	3.5	4.5	V
Drain cut-off current	I_{DSS}	V_{DS}=650 V, V_{GS}=0 V,T_j = 25°C	-	-	0.6	μA
Gate leakage current, Forward	I_{GSSF}	V_{GS}=30 V, V_{DS}=0 V	-	-	100	nA
Gate leakage current, Reverse	I_{GSSR}	V_{GS}=-30 V, V_{DS}=0 V	-	-	-100	nA
Drain-source on-state resistance	$R_{DS(on)}$	V_{GS}=10 V, I_D=12.5 A T_j = 25°C T_j = 150°C	- - -	 0.113 0.295	 0.125 -	Ω
Gate resistance	R_G	f=1 MHz, open drain	-	1.4	-	Ω
Dynamic characteristics						
Input capacitance	C_{iss}	V_{DS} = 100 V, V_{GS} = 0 V,	-	2235	-	pF
Output capacitance	C_{oss}	f = 250 kHz	-	79	-	
Reverse transfer capacitance	C_{rss}		-	1.4	-	
Turn-on delay time	$t_{d(on)}$	V_{DD} = 400V, I_D = 12.5A	-	17.4	-	ns
Rise time	t_r	R_G = 10Ω, V_{GS}=15V	-	9	-	
Turn-off delay time	$t_{d(off)}$		-	90	-	
Fall time	t_f		-	7	-	
Gate charge characteristics						
Gate to source charge	Q_{gs}	V_{DD}=520 V, I_D=12.5A,	-	10.2	-	nC
Gate to drain charge	Q_{gd}	V_{GS}=0 to 10 V	-	13.6	-	
Gate charge total	Q_g		-	43	-	
Gate plateau voltage	$V_{plateau}$		-	5	-	V
Reverse diode characteristics						
Diode forward voltage	V_{SD}	V_{GS}=0 V, I_F=12.5A	-	1.2	-	V
Reverse recovery time	t_{rr}	V_R=400 V, I_F=12.5A,	-	340	-	ns
Reverse recovery charge	Q_{rr}	dI_F/dt=100 A/μs	-	5.1	-	μC
Peak reverse recovery current	I_{rrm}		-	30	-	A

Notes:

1. Limited by maximum junction temperature, maximum duty cycle is 0.75.

2. I_{AS} = 5A, L=55mH,V_{DD} = 60V, Starting T_j= 25°C.

3: The value of R_{thJA} is measured by placing the device in a still air box which is one cubic foot.

Electrical Characteristics Diagrams

Figure 1. Typ. Output Characteristics

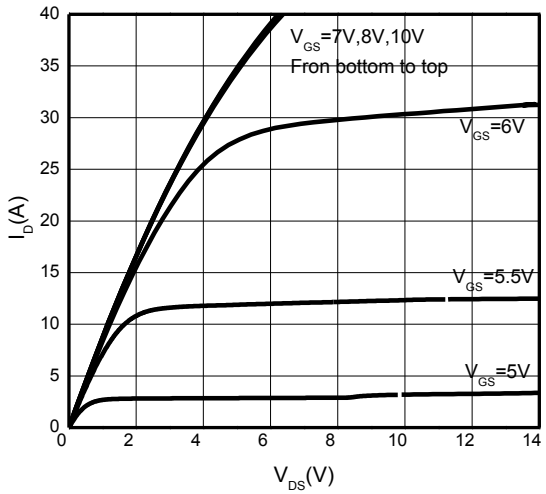


Figure 2. Transfer Characteristics

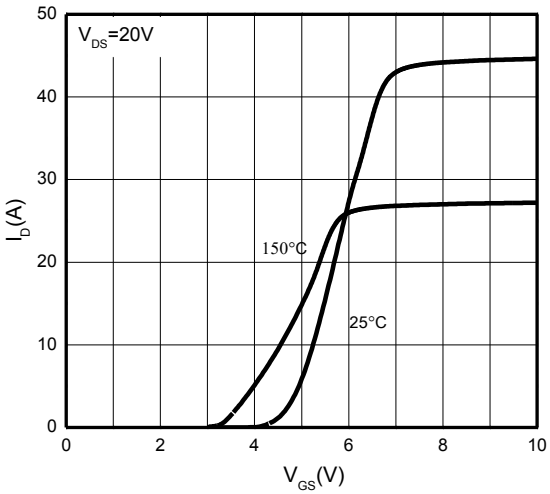


Figure 3. On-Resistance vs. Drain Current

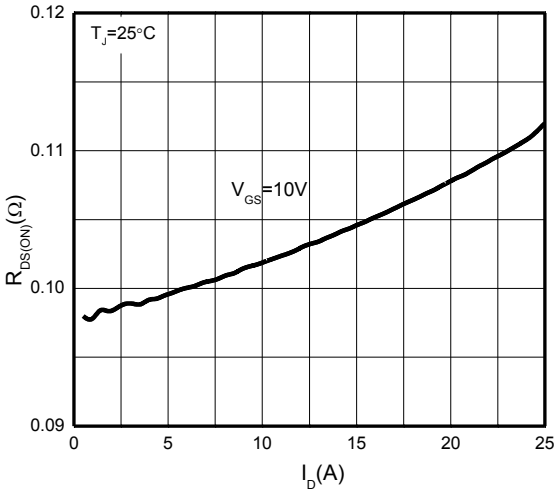


Figure 4.On-Resistance vs.Temperature

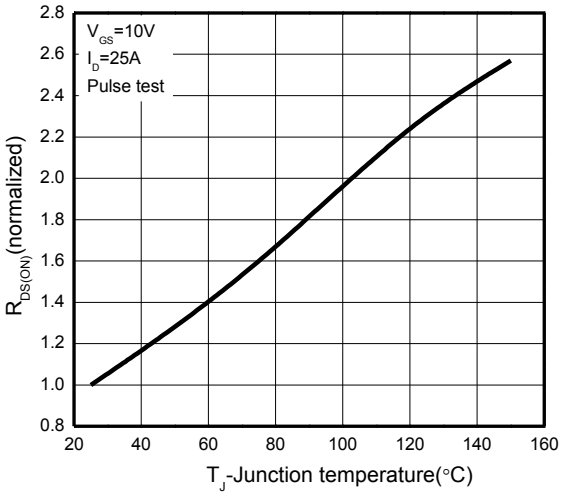


Figure 5.Breakdown Voltage vs.Temperature

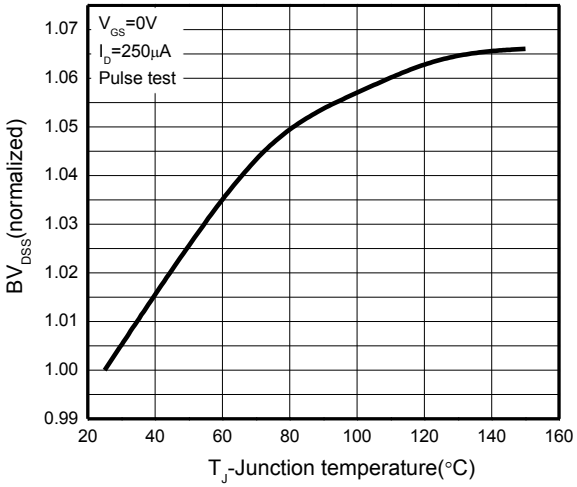


Figure 6.Threshold Voltage vs.Temperature

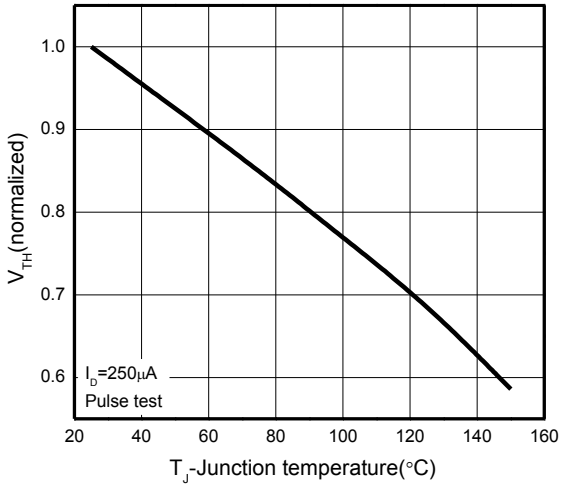


Figure 7.Body-Diode Characteristics

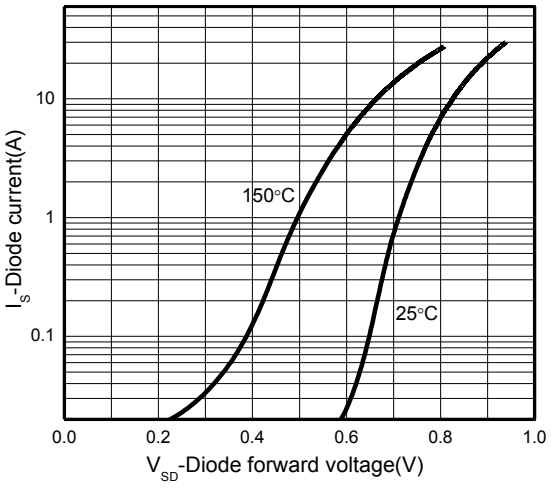


Figure 8.Capacitance Characteristics

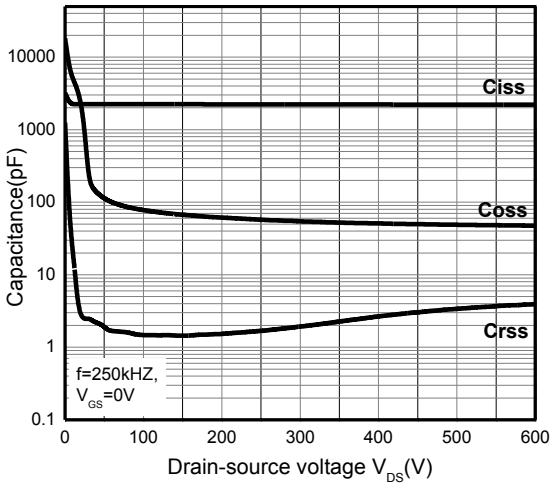


Figure 9.Gate Charge Characteristics

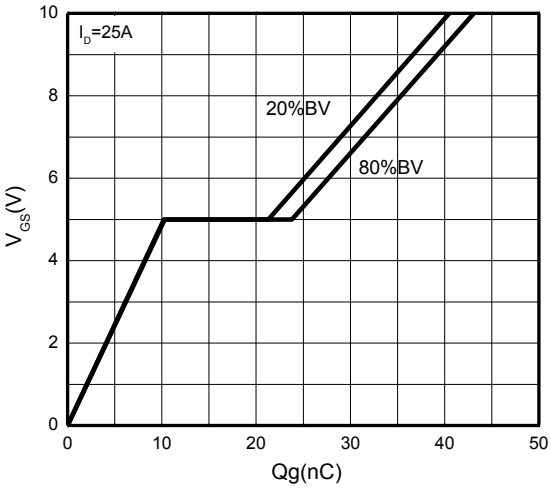


Figure 10.Drain Current Derating

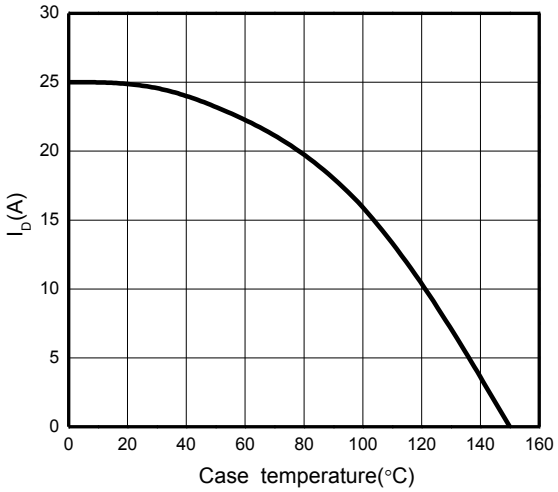


Figure 11.Power Dissipation vs.Temperature

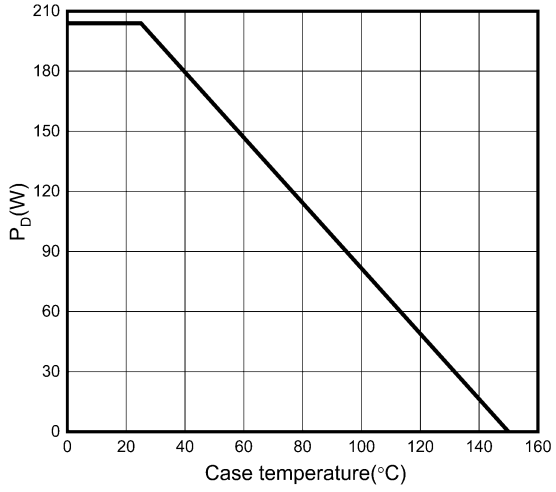


Figure 12: Safe Operating Area

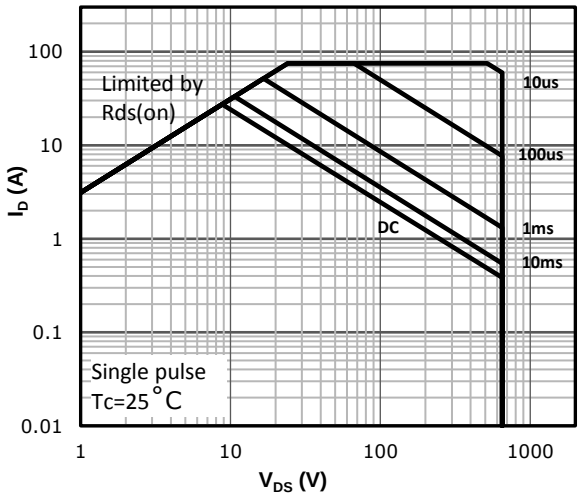
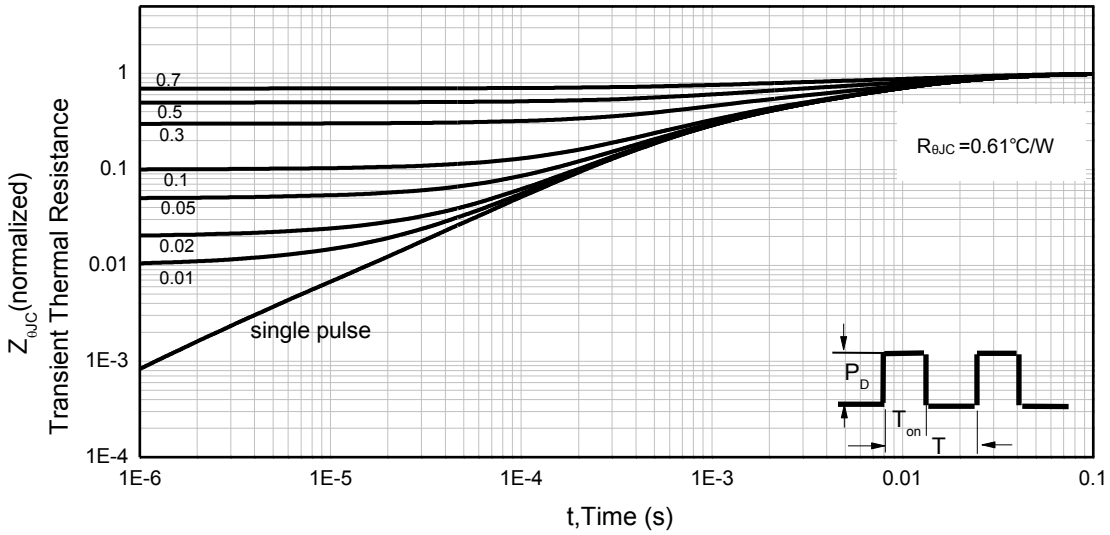
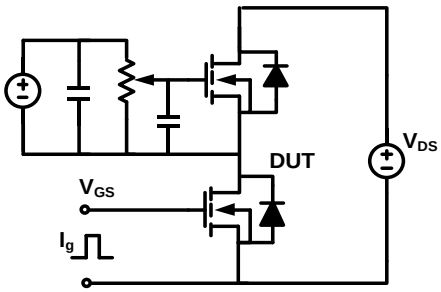


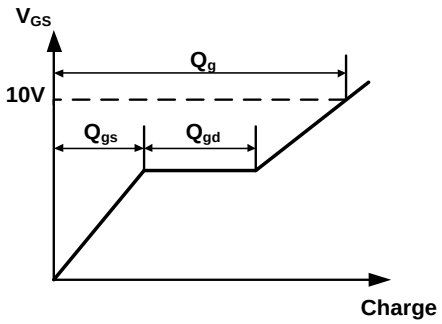
Figure 13. Normalized Maximum Transient Thermal Impedance (RthJC)



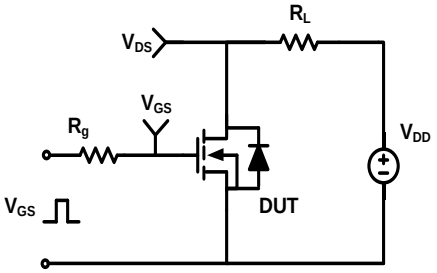
Test Circuit & Waveforms

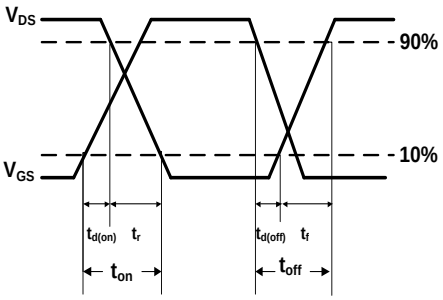
Gate Charge Test Circuit & Waveform



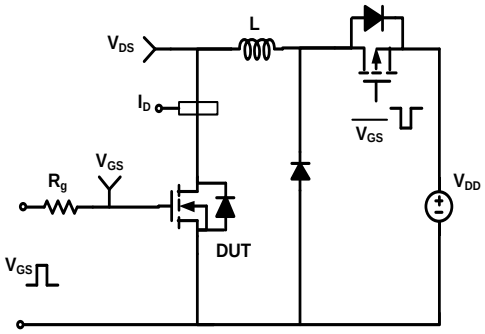


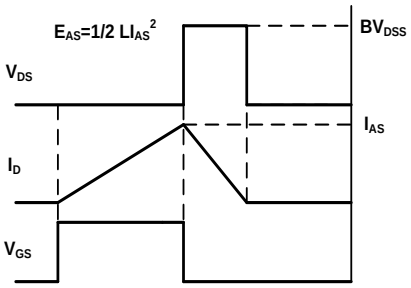
Resistive Switching Test Circuit & Waveform



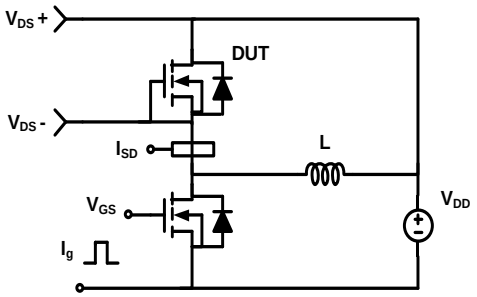


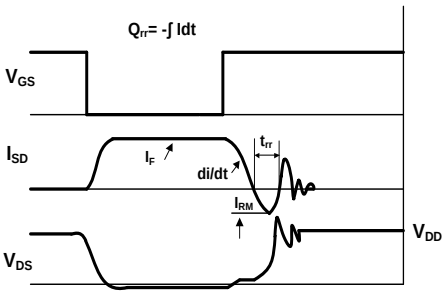
Unclamped Inductive Switching (UIS) Test Circuit & Waveform



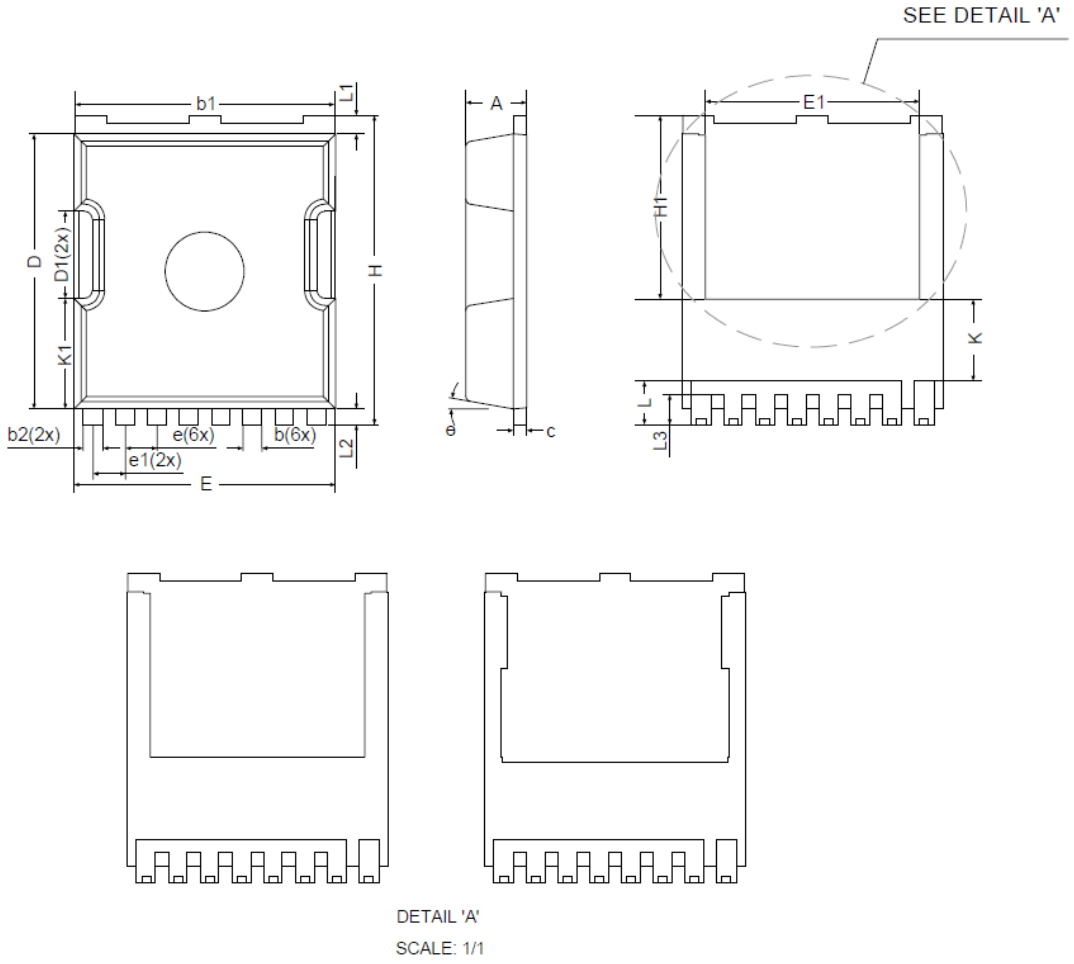


Diode Recovery Test Circuit & Waveform





Mechanical Dimensions for TOLL



SYMBOLS	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.15	2.45	0.085	0.096
b	0.60	0.90	0.024	0.035
b1	9.65	9.95	0.380	0.392
b2	0.65	0.90	0.026	0.035
c	0.40	0.60	0.016	0.024
D	10.18	10.58	0.401	0.417
D1	3.15	3.45	0.124	0.136
E	9.70	10.10	0.382	0.398
E1	7.90	8.40	0.311	0.331
e	1.10	1.30	0.043	0.051
e1	1.10	1.30	0.043	0.051
H	11.48	11.88	0.452	0.468
H1	6.75	7.30	0.266	0.287
K	2.45	3.33	0.096	0.131
K1	4.03	4.33	0.159	0.170
L	1.50	2.10	0.059	0.083
L1	0.50	0.90	0.020	0.035
L2	0.45	0.75	0.018	0.030
L3	1.00	1.30	0.039	0.051
θ	10° REF		10° REF	

Version Information

LST65R125HT
Revision 1.0

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